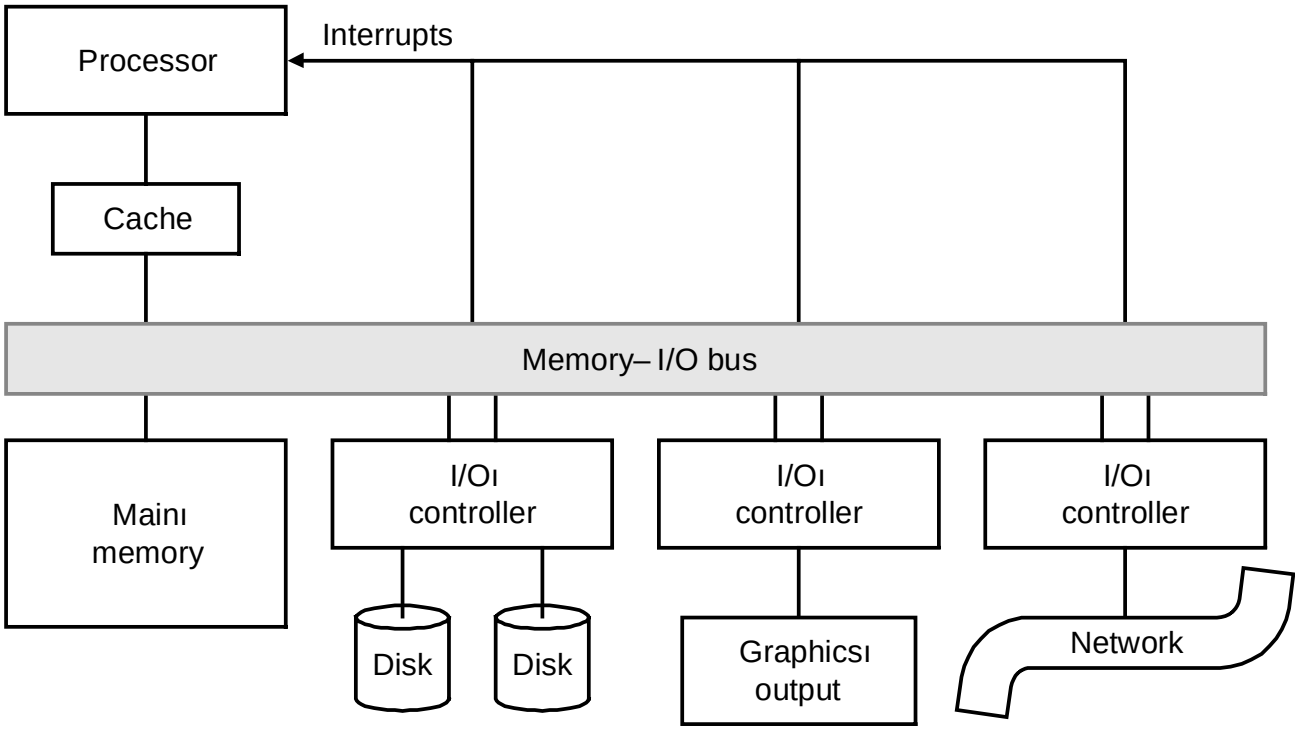
Interfacing Processors and Peripherals

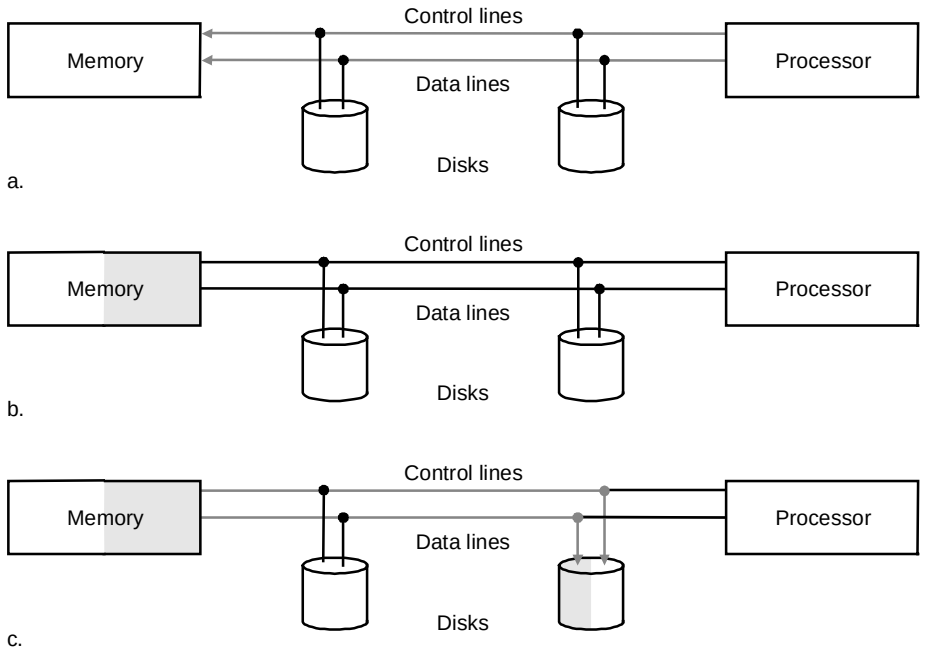


Buses

- Bus lines
  - Control lines
  - Data lines (data, commands, addresses)
- Bus transactions
  - Read (output): memory to I/O device
  - Write (input): I/O device to memory
- Types of buses
  - Processor-memory (specific)
  - I/O buses (standard)
  - Backplane bases (standard)

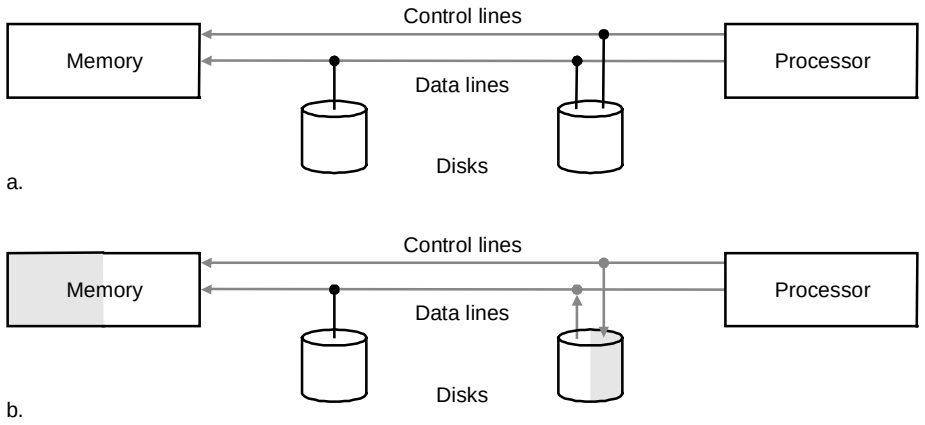
Bus transactions: output

- Request a read on control lines and supply data at the data lines
- Memory access
- Memory signals data availability and transfer them on the data line to I/O

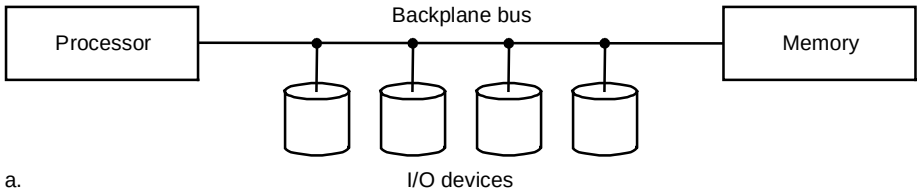


Bus transactions: input

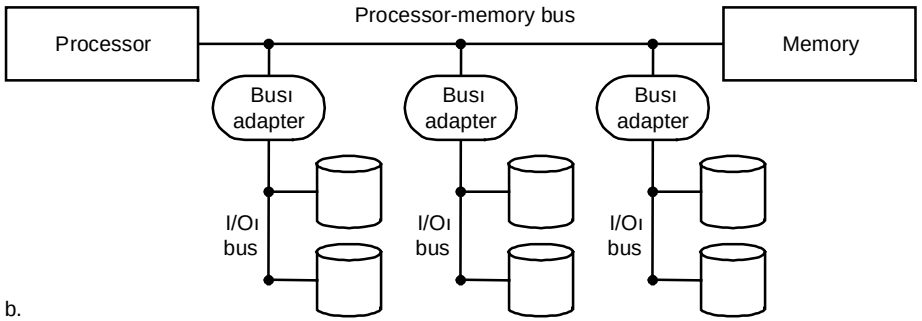
- Write request for memory on the control lines and address on the data lines
- Memory signal the I/O device that is ready and transfers starts



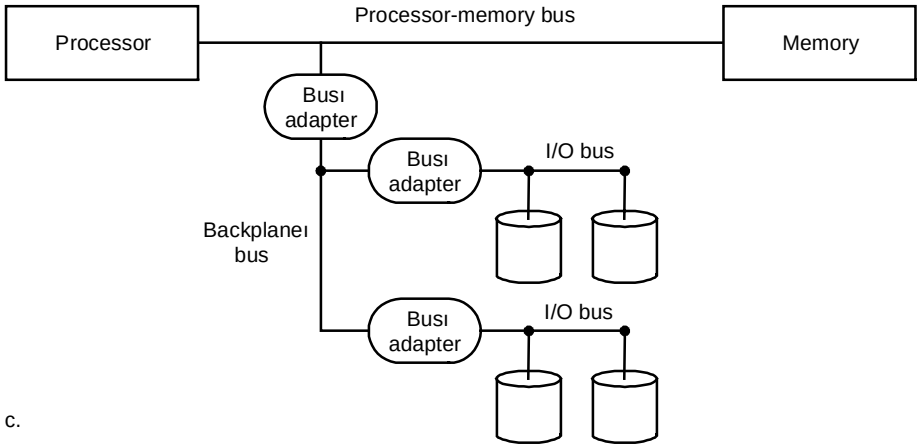
Types of buses



a.



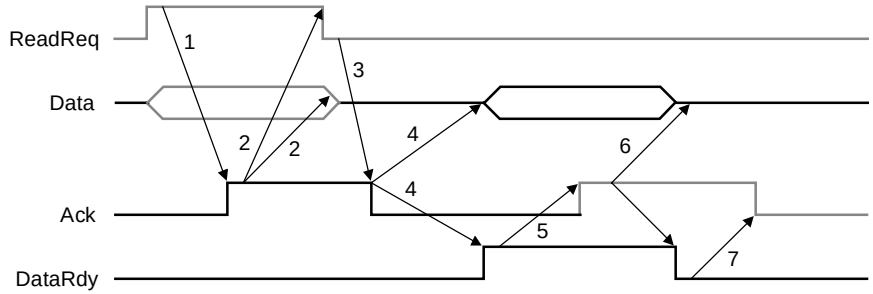
b.



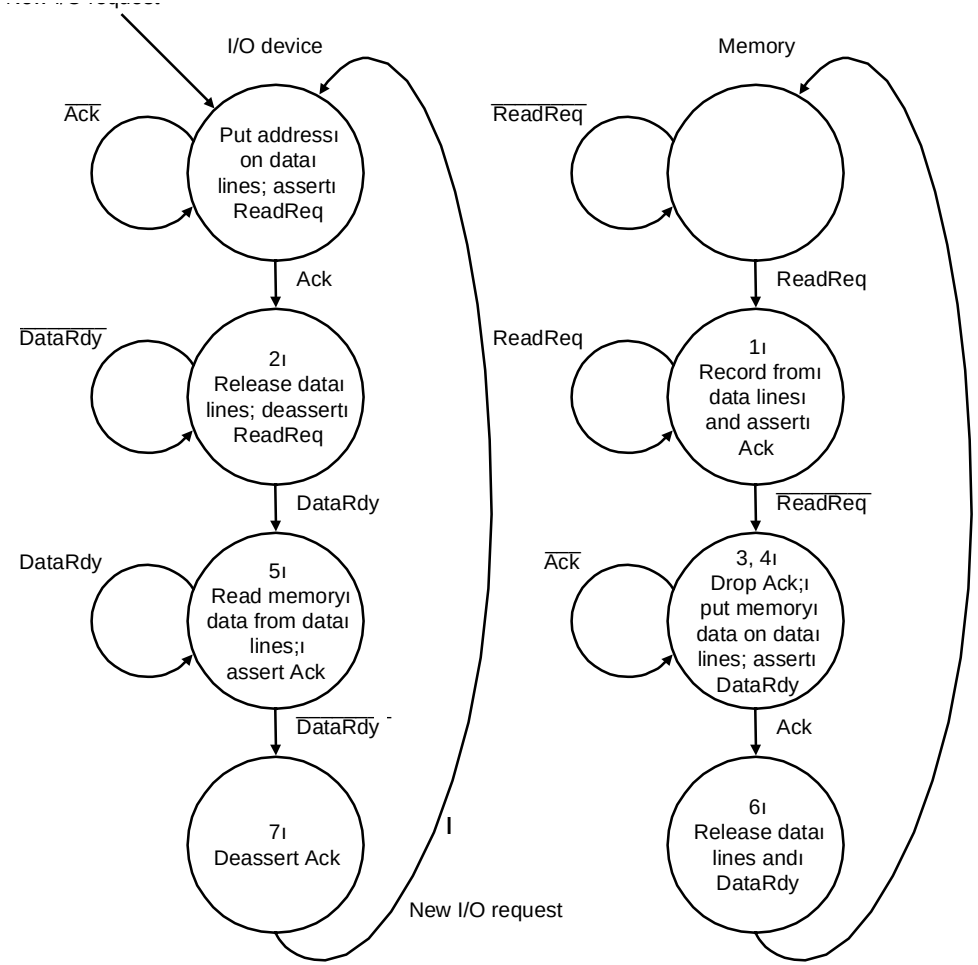
c.

Synchronous and Asynchronous buses

- Synchronous buses: Using a clock synchronized communication protocol
  - All devices use a single clock
  - Cannot be long
- Asynchronous buses: handshaking protocol
  - Reading a word from memory:
    - Read request (*ReadReq*)
    - Data are ready to read (*DataRdy*)
    - Acknowledge the ReadReq and DataRdy signals of the other party (*Ack*)



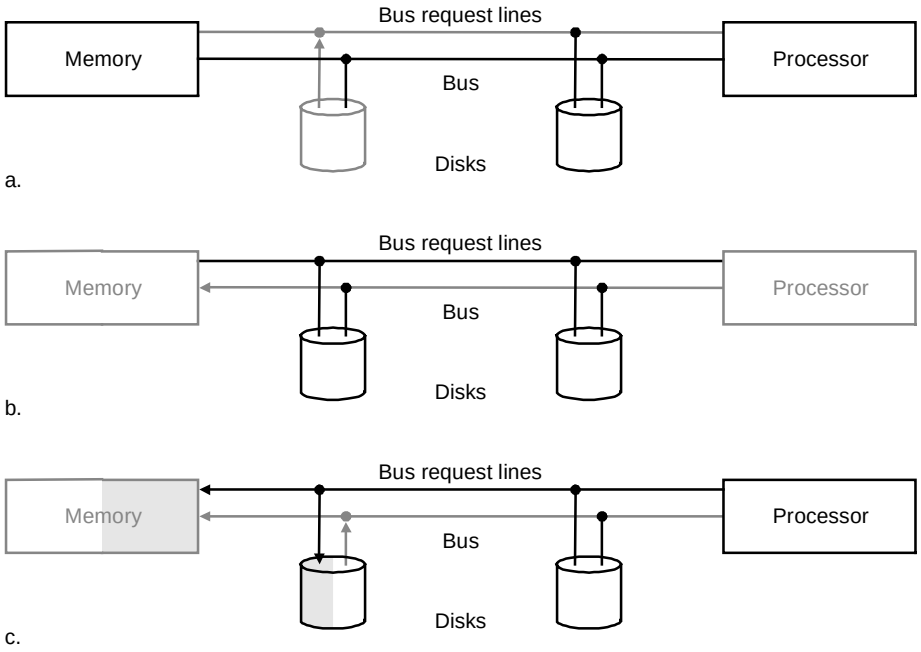
Implementing handshaking



Increasing the bus bandwidth

- Increasing the width of the data bus lines
- Using separate address and data lines
- Transferring multiple words (blocks)

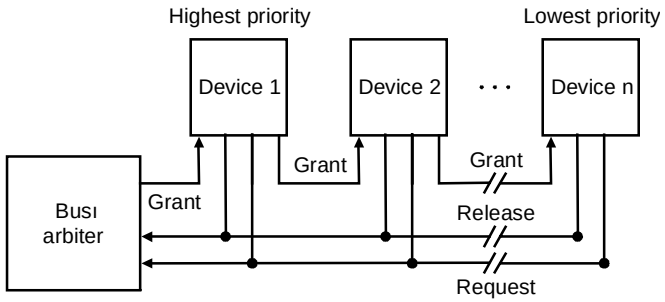
Bus access: master and slave



- I/O device generates a request to the processor to use the bus
- The processor responds and generates the corresponding bus control signals
- The processor notifies the device and the device places the address on the bus

Bus arbitration schemes

•**Daisy chain arbitration:** A single bus grant line is run through the devices from highest priority to lowest. A higher priority device intercepts the bus grant signal, not allowing a lower priority device to see it.
•**Centralized, parallel arbitration:** Using multiple request lines managed by a centralized arbiter.
•**Distributed arbitration by self-selection:** Multiple request lines, but the device requesting the bus access determine who will be granted access. Each bus requesting device places its identity code on the bus.
•**Distributed arbitration by collision detection:** Each device independently requests the bus. Multiple simultaneous requests result in a collision, which is detected and solved.



Bus standards

Characteristic	**PCI**	**SCSI**
Type	Backplane	I/O
Data bus width	32-64	8-32
Address/data multiplexed?	Yes	Yes
Number of bus masters	multiple	multiple
Arbitration	Centralized, parallel	Self-selection
Clocking	Synchronous 33-66MHz	Asynchronous or synchronous 5-10MHz
Theoretical peak bandwidth	133-512 MB/sec	5-40 MB/sec
Estimated achievable bandwidth	80 MB/sec	2.5-40 MB/sec
Maximum number of devices	1024	7-31
Maximum bus length	0.5 meter	25 meters