Fig. 5-1 Block Diagram of Sequential Circuit
Combinational circuit

Inputs

Clock pulses

Outputs

(a) Block diagram

Fig. 5-2 Synchronous Clocked Sequential Circuit
SR Latch with NOR Gates

(a) Logic diagram

(b) Function table

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0  (after $S = 1, R = 0$)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1  (after $S = 0, R = 1$)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Fig. 5-3  SR Latch with NOR Gates
Fig. 5-4  SR Latch with NAND Gates

(a) Logic diagram  

(b) Function table

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q'</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
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<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Fig. 5-5 SR Latch with Control Input

<table>
<thead>
<tr>
<th>$C$</th>
<th>$S$</th>
<th>$R$</th>
<th>Next state of $Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>$Q = 0$; Reset state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>$Q = 1$; set state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Indeterminate</td>
</tr>
</tbody>
</table>
(a) Logic diagram

(b) Function table

<table>
<thead>
<tr>
<th>$C$</th>
<th>$D$</th>
<th>Next state of $Q$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>No change</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$Q = 0$; Reset state</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$Q = 1$; Set state</td>
</tr>
</tbody>
</table>

Fig. 5-6  D Latch
Fig. 5-7 Graphic Symbols for Latches

Sr

Sr

D
Fig. 5-8  Clock Response in Latch and Flip-Flop
Fig. 5-9 Master-Slave D Flip-Flop
Fig. 5-10  $D$-Type Positive-Edge-Triggered Flip-Flop
Fig. 5-11  Graphic Symbol for Edge-Triggered D Flip-Flop

(a) Positive-edge

(a) Negative-edge
Fig. 5-12  *JK* Flip-Flop

(a) Circuit diagram

(b) Graphic symbol
Fig. 5-13  T Flip-Flop

(a) From $JK$ flip-flop

(b) From $D$ flip-flop

(c) Graphic symbol
Fig. 5-14  D Flip-Flop with Asynchronous Reset
Fig. 5-15  Example of Sequential Circuit
Fig. 5-16  State Diagram of the Circuit of Fig. 5-15
Fig. 5-17 Sequential Circuit with $D$ Flip-Flop
Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

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Fig. 5-19 State Diagram of the Circuit of Fig. 5-18
Fig. 5-20  Sequential Circuit with $T$ Flip-Flops

(a) Circuit diagram

(b) State diagram

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Fig. 5-21  Simulation Output of HDL Example 5-7
Fig. 5-22 State Diagram
Fig. 5-23  Reduced State Diagram
Fig. 5-24 State Diagram for Sequence Detector
Fig. 5-25  Maps for Sequence Detector

\[ D_A = A_x + B_x \]
\[ D_B = A_x + B'_x \]
\[ y = AB \]
Fig. 5-26  Logic Diagram of Sequence Detector
Fig. 5-27 Maps for $J$ and $K$ Input Equations

$J_A = Bx'$

$K_A = Bx$

$J_B = x$

$K_B = (A \oplus x)'$
Fig. 5-28 Logic Diagram for Sequential Circuit with JK Flip-Flops
Fig. 5-29  State Diagram of 3-Bit Binary Counter
Fig. 5-30 Maps for 3-Bit Binary Counter

\[ T_{A2} = A_1 A_0 \]

\[ T_{A1} = A_0 \]

\[ T_{A0} = 1 \]
Fig. 5-31  Logic Diagram of 3-Bit Binary Counter
Fig. P5-7
Fig. P5-8
Fig. P5-19