Combinational circuit

Fig. 4-1 Block Diagram of Combinational Circuit
Fig. 4-2 Logic Diagram for Analysis Example
Fig. 4-3  Maps for BCD to Excess-3 Code Converter
Fig. 4-4 Logic Diagram for BCD to Excess-3 Code Converter
Fig. 4-5 Implementation of Half-Adder

(a) \( S = x y' + x' y \)  
\( C = xy \)

(b) \( S = x \oplus y \)  
\( C = xy \)
\[ S = x'y'z + x'yz' + xy'z' + xyz \]

\[ S = xy + xz +yz \\
    = xy + xy'z + x'y'z \]

Fig. 4-6 Maps for Full Adder
Fig. 4-7  Implementation of Full Adder in Sum of Products
Fig. 4-8 Implementation of Full Adder with Two Half Adders and an OR Gate
Fig. 4-9 4-Bit Adder
Fig. 4-10 Full Adder with P and G Shown
Fig. 4-11 Logic Diagram of Carry Lookahead Generator

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Fig. 4-12 4-Bit Adder with Carry Lookahead
Fig. 4-13 4-Bit Adder Subtractor
Fig. 4-14 Block Diagram of a BCD Adder
Fig. 4-15  2-Bit by 2-Bit Binary Multiplier
Fig. 4-16 4-Bit by 3-Bit Binary Multiplier
Fig. 4-17  4-Bit Magnitude Comparator
Fig. 4-18 3-to-8-Line Decoder

\[ D_0 = x'y'z' \]
\[ D_1 = x'y'z \]
\[ D_2 = x'yz' \]
\[ D_3 = x'yz \]
\[ D_4 = xy'z' \]
\[ D_5 = xy'z \]
\[ D_6 = xyz' \]
\[ D_7 = xyz \]
Fig. 4-19 2-to-4-Line Decoder with Enable Input
Fig. 4-20  $4 \times 16$ Decoder Constructed with Two $3 \times 8$ Decoders
Fig. 4-21 Implementation of a Full Adder with a Decoder
Fig. 4-22 Maps for a Priority Encoder

\[ x = D_2 + D_3 \]

\[ y = D_3 + D_1D'_2 \]
Fig. 4-23 4-Input Priority Encoder
Fig. 4-24  2-to-1-Line Multiplexer

(a) Logic diagram

(b) Block diagram
(a) Logic diagram

<table>
<thead>
<tr>
<th>$s_1$</th>
<th>$s_0$</th>
<th>$Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>$I_0$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>$I_1$</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>$I_2$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>$I_3$</td>
</tr>
</tbody>
</table>

(b) Function table

Fig. 4-25 4-to-1-Line Multiplexer
Fig. 4-26  Quadruple 2-to-1-Line Multiplexer

Function table

<table>
<thead>
<tr>
<th>$E$</th>
<th>$S$</th>
<th>Output $Y$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$X$</td>
<td>all 0's</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>select $A$</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>select $B$</td>
</tr>
</tbody>
</table>

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Fig. 4-27 Implementing a Boolean Function with a Multiplexer

<table>
<thead>
<tr>
<th>$x$</th>
<th>$y$</th>
<th>$z$</th>
<th>$F$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
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<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

(a) Truth table

(b) Multiplexer implementation

$F = z$

$F = z'$

$F = 0$

$F = 1$
Fig. 4-28  Implementing a 4-Input Function with a Multiplexer
Normal input $A$  
Output $Y = A$ if $C = 1$
High-impedance if $C = 0$
Control input $C$

Fig. 4-29  Graphic Symbol for a Three-State Buffer
(a) 2-to-1 line mux

(b) 4-to-1 line mux

Fig. 4-30 Multiplexers with Three-State Gates
Fig. 4-31 Three-State Gates
Fig. 4-32  2-to-1-Line Multiplexer with Three-State Buffers
Fig. 4-33  Stimulus and Design Modules Interaction
Fig. P4-1
(a) Segment designation

(b) Numerical designation for display

Fig. P4-9
Fig. P4-17 First Stage of a Parallel Adder